



## ML4003BX BERT | User Guide

Installation | Connection | Measurement

User Manual Revision 1.0, October 2021



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Only qualified personnel should perform service procedures.

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**Do Not Operate in Wet/Damp Conditions. Do Not Operate in an Explosive Atmosphere. Keep Product Surfaces Clean and Dry**



*Caution statements identify conditions or practices that could result in damage to this product or other property.*

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**Error! Bookmark not defined.**

## Revision Control

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Revision number	Description
1.0.0	<ul style="list-style-type: none"><li>Initial Release, SW rev. 1.0 (HD)</li></ul>
1.1.0	<ul style="list-style-type: none"><li>SW rev. 4.0.0</li></ul>

## List of Acronyms

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Acronym	Definition
BW	Bandwidth
BERT	Bit Error Rate Tester
Conf	Configuration
DUT	Device Under Test
FEC	Forward Error Correction
FW	Firmware
GBd	Giga Baud
Gbps	Gigabits per second
GUI	Graphical User Interface
HW	Hardware
ISI	Inter-symbol Interference
JTOL	Jitter Tolerance
NRZ	Non-Return to Zero
PAM4	Pulse Amplitude Modulation (4-level)
SI	Signal Integrity
SNR	Signal-to-Noise Ratio
Sim	Simulation
SW	Software

## Introduction

---

The ML4003BX is a state of the art, low cost PON tester consisting of a BERT, Digital Sampling Oscilloscope and an optical scope, all integrated in a compact 2U cPCI form factor. It supports burst mode PON by providing a programmable AWG output that can be programmed by the user to output a custom 64 bit TTL signal, synchronous to the high-speed data. The ML4003BX can be ordered as a low cost 16 Gbps Bit Error Ratio Tester with 32 GHz DSO and can be expanded to include a 10G / 25GHz Optical sampling scope. The full-fledged configuration contains in addition to the BERT, a 32 GHz (50GHz optionally) DSO, one SFP28 or one XFP port in addition to a 25 GHz (Optionally 10 GHz for a lower cost) optical sampling oscilloscope.

In the following user manual, a detailed explanation is provided to cover the installation, calibration and measurements performed on the ML4003BX.

## Installation

To install and start using the TDA interface for the first time, follow this step-by-step installation guide (with pictures) below:

1. **Run** the TDA setup file.
2. **Install** TDA.
3. **Connect** the ML BERT to the local network.
4. **Launch** the GUI.
5. **Start** the measurements.

After downloading the TDA setup file, select run and follow this easy step-by-step installation procedure:

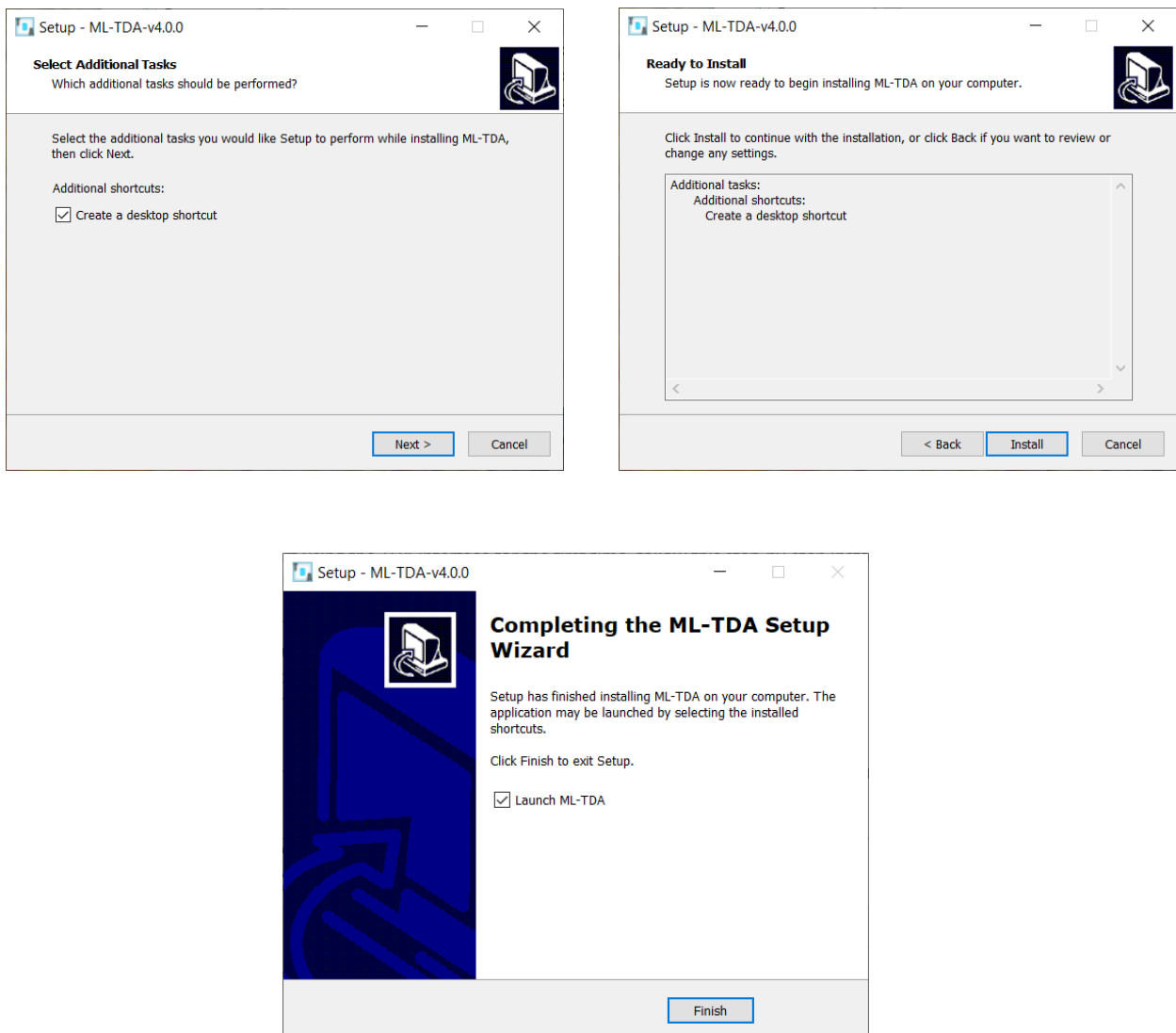


Figure 1 GUI Installation



TDA should now be ready to run, with a shortcut button on the Desktop.

## Connecting to the Instrument

To connect to the instrument, follow this sequence of steps:

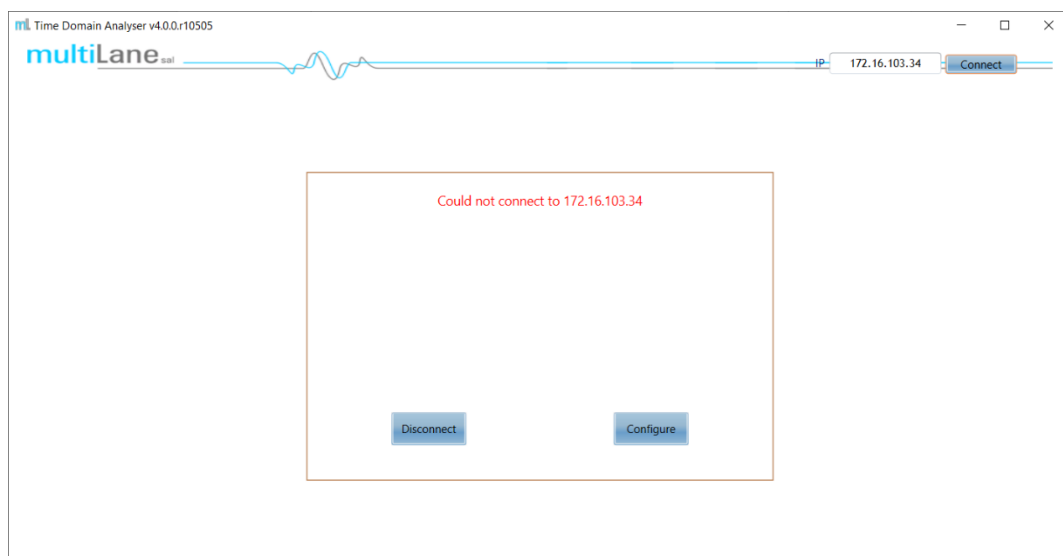
- **Install** the ML-TDA GUI software.
- **Plug** the ML4003BX in the chassis.
- **Power Up** the ML4003BX.
- **Connect** the device to the network\* using a RJ45/LAN cable.  
*LAN connection can be validated with a ping to the static instrument IP.*
- **Run** ML-TDA software.
- **Connect** using the IP address of the target instrument(s) (Figure 2). The IP address is printed on the back side of the instrument.



Figure 2 Connection Window

### NOTES:

- In the case of a connection failure, a pop-up message will appear indicating a connection error (Figure 3).



*Figure 3 Connection Failure*

\*To add the device to the network, consult [Appendix I](#) at the end of this manual

## Connection

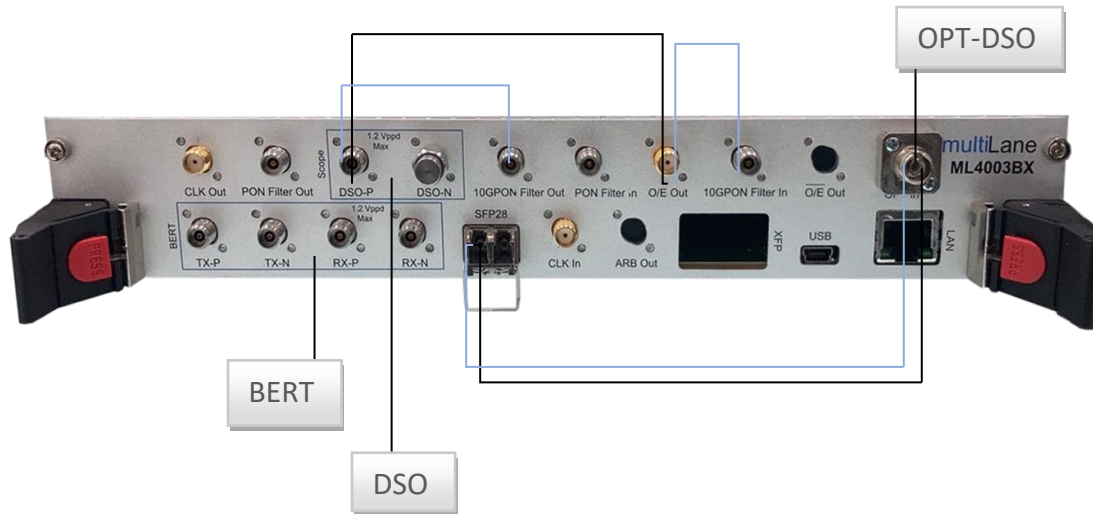


Figure 4 ML4003BX Faceplate

### BERT Connections

To use the ML4003BX as a BERT, connect to the BERT pins.

- **TX-P and TX-N** are the transmitter pins
- **RX-P and RX-N** are the receiver pins

To use SFP28 or XFP transceiver, plug the transceiver in its corresponding port.

**CLK Out** is used when the user wants to generate a clock from the ML4003BX BERT.

### DSO Connections

#### 1. Electrical DSO

To use the ML4003BX as an electrical DSO, connect to DSO-P and DSO-N pins.

#### 2. Optical DSO

To use the ML4003BX as an optical DSO:

- Connect optical cable to OPT In
- Connect O/E out to DSO-P or DSO-N and terminate the unconnected port with a 50 ohms termination (*refer to the black lines in figure 4*)

- To use PON or 10GPON filters, connect O/E out to PON Filter in or 10GPON Filter in, then connect PON Filter out or 10GPON Filter out to DSO-P or DSO-N and terminate the unconnected port (*refer to the blue lines in figure4*)

**CLK In** is used when the user wants to use an external clock.

## Measurement

Once connected to the instrument and the GUI, the ML4003BX can be configured as a BERT or DSO (Optical or Electrical) or BERT and DSO simultaneously.

### BERT Configuration

In order to use ML4003BX as a BERT, select BERT from the main window and click on configure.



Figure 5 BERT configuration

After configuring the instrument, run the desired configuration from the configuration window (Figure 5).

1. **Select** line Rate
2. **Configure** Clock Out
3. **Set** PRBS

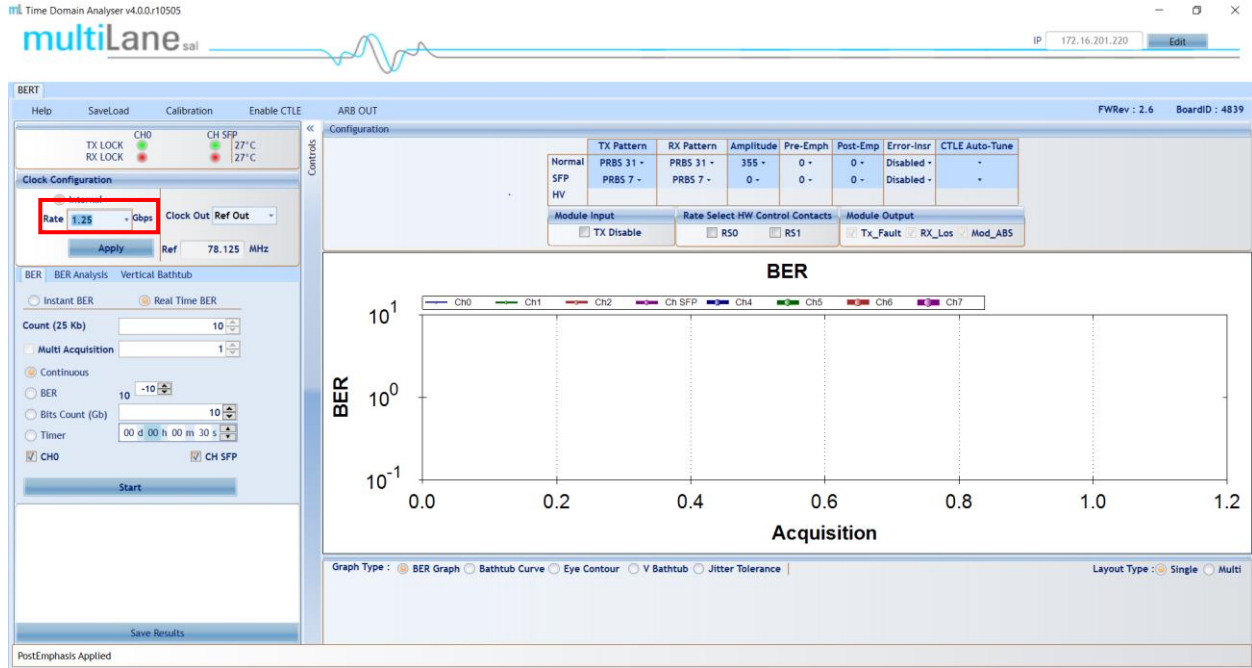


Figure 6 Rate Selection

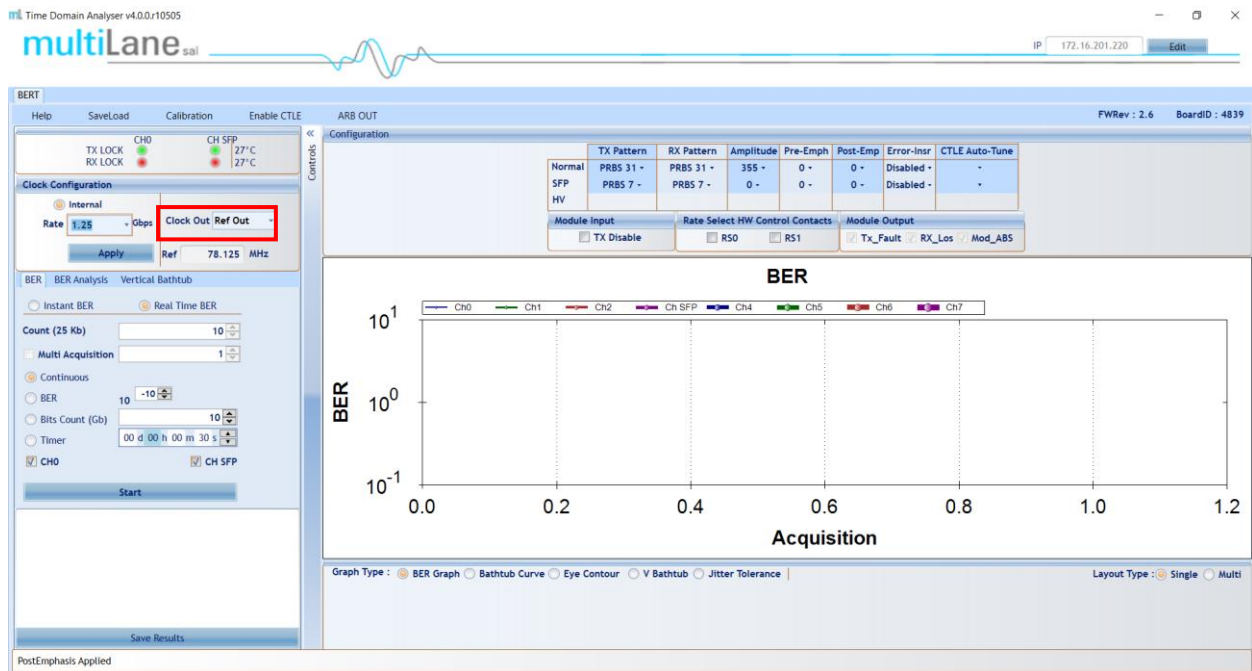


Figure 7 Clock Configuration

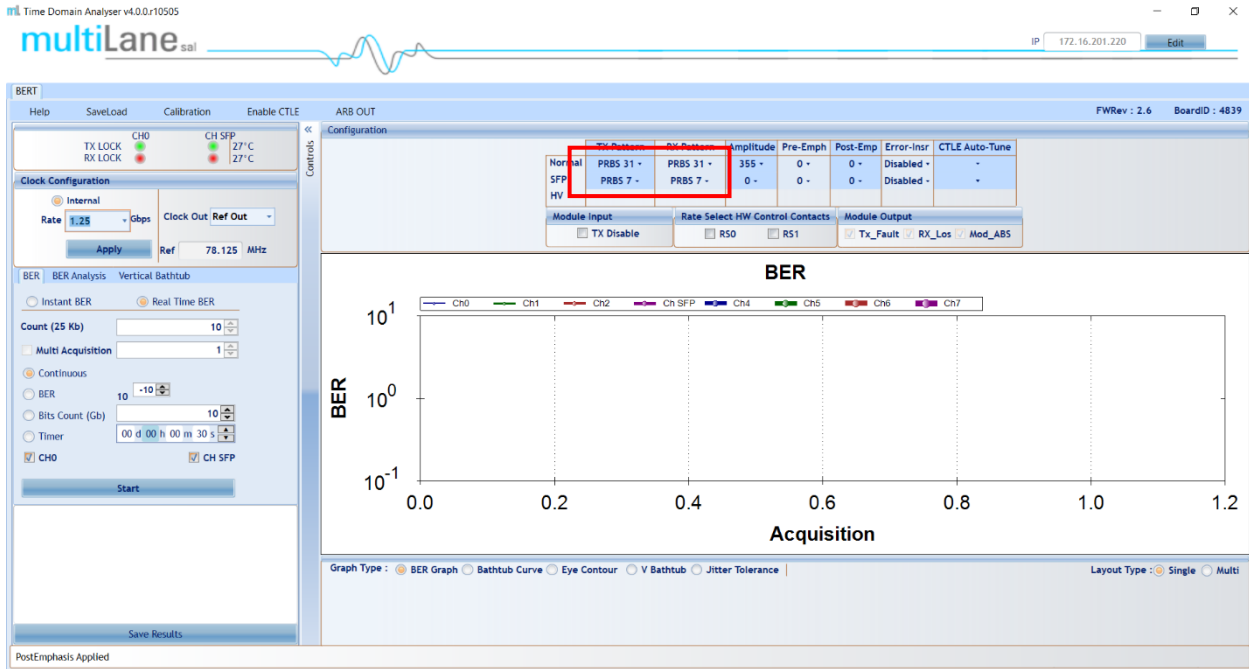


Figure 8 PRBS setting

\*Note that Normal is selected when using the BERT ports and SFP is selected when using SFP Port

## PRBS Pattern Configuration

- In the PRBS Configuration group box, select the pattern required; the available patterns are 7, 9, 15, 23, 31 and sinusoidal in addition to the 40 bits user pattern. TX Pattern tab is used for Configuring Generated signal, RX Pattern tab is used for pattern verification.
- To use the User defined capability, first select it from the Pattern combo box list, then in the text box specified for the User Defined write the sequence of bits you want. The sequence of bits should be in Hexadecimal only (16 bits length), ie FF, and then click the Set button.
- To make the TX off, choose the TX OFF
- In case the test engineer wired the positive TX channel to the negative RX channel by mistake, the software can compensate for this error by clicking on the invert button.

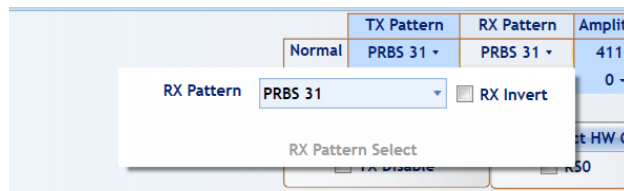


Figure 9 PRBS configuration

The specified generator now starts generating a clean signal. If you would like to inject jitter to the signal generated to start shaping the eye diagram, you have to adjust the slide bars existing in the Eye Shaping group box (refer to the section Eye Shaping)

## Eye Shaping

This instrument includes 3 sliders to shape the form of the eye diagram, amplitude, Pre-emphasis and Post-emphasis. All slider values and other configurations are saved in the EPROM:

- **Amplitude** TX output amplitude is between 0mV and 800mV.
- **Pre Emphasis** TX output Pre-emphasis amplitude value could be changed from 0 to 15%.
- **Post Emphasis** TX output Signal Post-emphasis amplitude value could be changed from 0 to 31%.

Amplitude	Pre-Emph	Post-Emp
520 ▾	15 ▾	31 ▾
0 ▾	15 ▾	31 ▾

Figure 10 Eye Shaping sliders

## Error Insertion

Error-Insr tab allows configuring signal error insertion. Rate select list allows the user to choose the amount of error bits. Rate will vary between 1 and 40 bits. Continuous checkbox allows continuously inserting error to the generated signal.

Rate  bits

Continuous

Error Insertion

Figure 11 Error insertion



## CTLE Configuration

CTLE Tab allows the user to select the equalization level; CTLE varies from 0 to 10 dB to compensate for cable loss from the DUT to the BERT and to de-embed the system losses.

The auto adapt selects the best CTLE mode

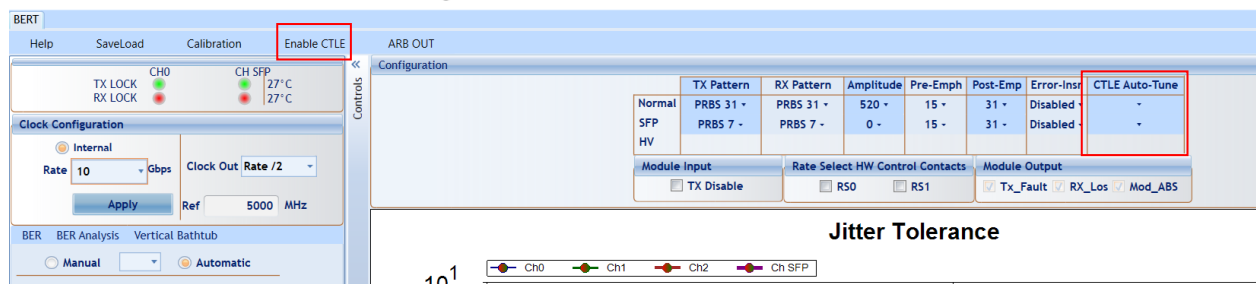


Figure 12 CTLE

## Bit Error Ratio Reading

To be able to start BER measurements, the instrument ports should be in the loopback mode, which means TX port should be connected to the RX port.

To monitor the BER function, we have dedicated an LED to make sure it is locked.

- If the LED is green that means the RX is locked to the incoming data.
- If the LED is red that means the RX is not locked to the incoming data, which means there is a possibility that the cables are not connected correctly, thus try the invert function at the TX and RX sides; if the problem persists check the connections of your cables. The patterns of the Detector are automatically

modified when you change the generator pattern value.

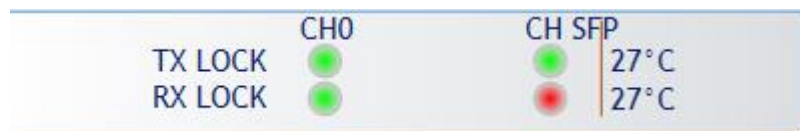


Figure 13 Channels LEDs: Lock on CH0

## BER

BER test has the following configuration:

- **Count (25kbit):** Number of packets to be collected
- **Repeat Count:** if selected it allows you to choose the number of acquisitions. The measurements will be for the preceding configuration.

The screenshot shows the configuration window for the BER test. It includes the following elements:

- Tabs: BER, BER Analysis, Vertical Bathtub
- Radio buttons:  Instant BER,  Real Time BER
- Count (25 Kb): 10
- Multi Acquisition:  1
- Radio buttons:  Continuous,  BER,  Bits Count (Gb),  Timer
- BER value: 10, Offset: -10
- Bits Count (Gb): 10
- Timer: 00 d 00 h 00 m 30 s
- Checkboxes:  CHO,  CH SFP
- Start button

Figure 14 BER test

## Real Time BER

This feature allows the BERT to collect Real Time BER.

- **Configuration Count (25kbit):** Number of packets to be collected.
- **Repeat Count:** if selected it allows you to choose the number of acquisitions.
- **Continuous BER:** the BER value is repeated after each set the packet counts.
- **BER:** The BER test will run till it reaches the amount of BER selected. **Timer:** The BER test will run for the specified amount of time.

## Jitter Tolerance Test

Our user friendly JTOL tool, allows the user to perform automatic jitter injection for the stressed input applications and for characterization. This tool is featured in the BERT GUI (v.3.0.r3784 and above, MLBert\_A.dll r 3783). The tool needs MultiLane' ML407 clock synthesizer (up to 60 MHz) for multi-UI sinusoidal jitter generation and the ML4003BX. This option facilitates 10/40/100Gbps stressed input compliance testing. If you have an ML4003BX, you can use it to test your DUT's tolerance to Sinusoidal Jitter by either letting the GUI execute the test automatically according to the limits specified for CAUI4 or XLAUI4, or by self-defining the frequencies at which the test should be executed and the pass/fail criteria.

### Modes of operation for the JTOL

Two modes of operation are featured and both require the clock synthesizer's input.

- **Automatic mode:** Features two masks, CAUI4 for high rate (25.78125Gbps) and XLAUI4 (10.3125Gbps) for low rate. Each test is performed based on the IEEE802.3bm- 2015 standards for high rate and IEEE802.3ba-2010 for low rate.
- **Manual mode:** The user can choose the desired frequency at which the sinusoidal jitter is generated, also specifying the desired UI interval.

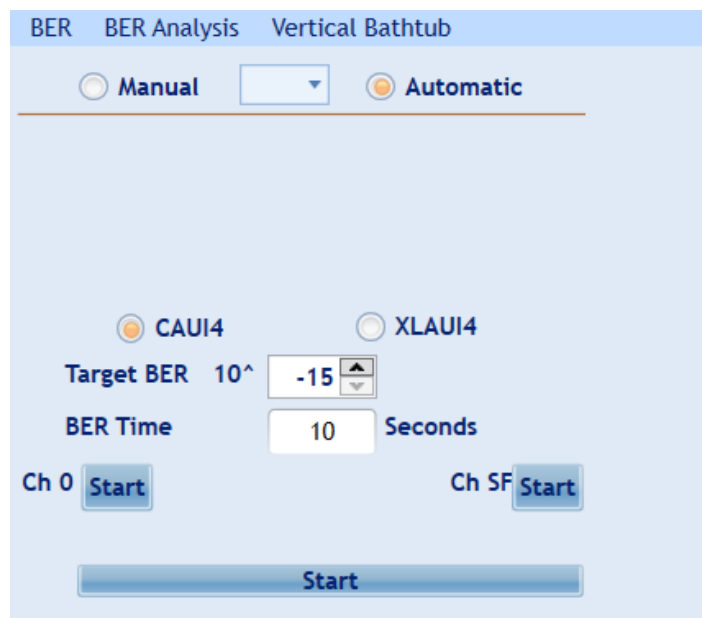


Figure 15 JTOL modes of operation

## Bit Error Ratio analysis

### *The Bathtub Plot*

A viewpoint of jitter is provided by a bathtub plot, so named because its characteristic curve looks like the cross section of a bathtub. It is a graph of BER versus sampling point throughout the unit interval. It is typically shown with a log scale, which illustrates the functional relationship of sampling time to bit error ratio. Also, the deep eye width can be entered to get the BER level. When the sampling point is at or near the transition points, the BER is 0.5 (equal probability for success or failure of a bit transmission). The curve is flat in these regions, which are dominated by deterministic jitter mechanisms. As the sampling point moves inward from both ends of the unit interval, the BER drops off precipitously. These regions are dominated by random jitter mechanisms and the BER is determined by the sigma of the Gaussian processes producing the random jitter. As expected, the center of the unit interval provides the optimum sampling point. Note that there is BER measured for the middle sampling times.

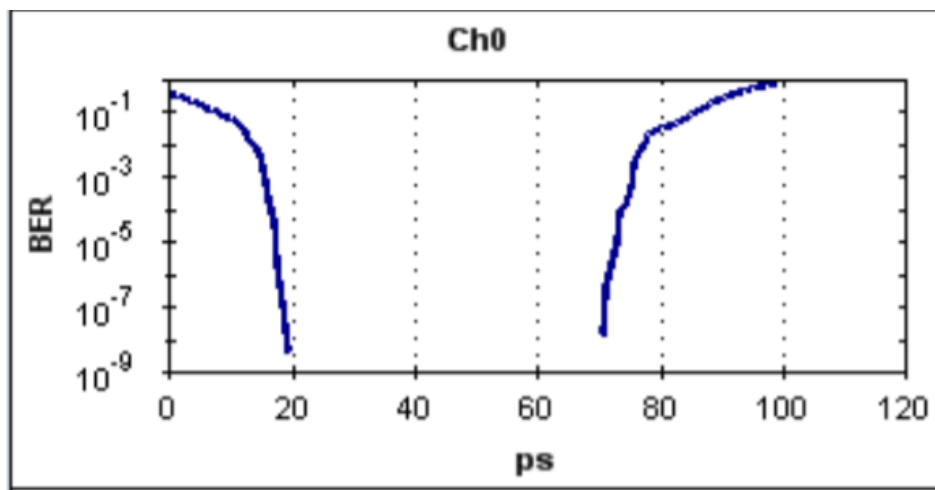


Figure 16 Bathtub plot

Plotting the points on a graph of BER versus sampling location in time results in a curve that resembles the cross section of a bathtub, hence the term bathtub curve. A bathtub curve can be created either by software extrapolation from voltage over time measurement done by an oscilloscope, or by actually sampling the bits as done by a BERT. For development engineers, the final proof of performance of a component or subsystem is the direct measurement of BER at optimized timing and threshold levels employing error detection on every transmitted bit. However, the speed of the BER measurement is a function of the BER to be measured and the desired statistical confidence factor for the result.

### Bathtub configuration

To run the bathtub you should set the following configuration:

- **Target BER:** Select which level the Bathtub will reach. Upon selection, estimation of the time will be given.

- **Full sweep:** Read the BER at every point and allow the user to choose the start and stop time for the scan (time in mS). You can select a channel at a time to measure the Bathtub.
- **Dual Dirac:** Doesn't allow the user to choose the start and stop time for the scan



Figure 17 Bathtub Configuration

## Eye Contour

### Eye Contour Configuration

To run the Eye Contour you should set the following configuration:

- **Accumulated:** Select the number of data acquisitions. Upon selection, estimation of the time will be given. You can select a channel at a time to do the Eye Contour measurements.

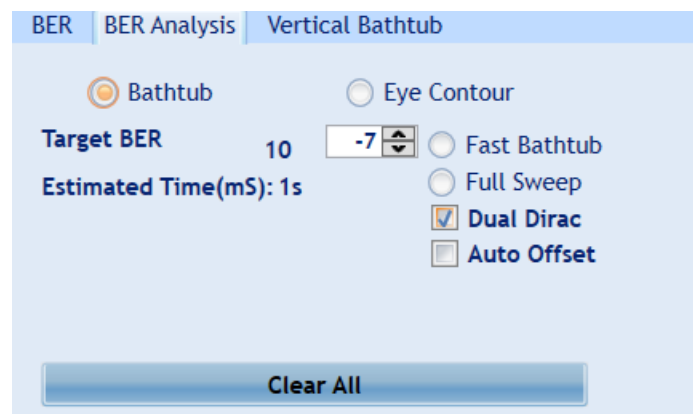


Figure 18 Eye Configuration

## Mask test

Masks typically represent an area in the eye opening that you want to ensure unit intervals do not fall within. The mask test is highly efficient since it quantifies both time and amplitude parameters in one measurement. The user should check the checkbox of the MASK to view the failing points, after specifying the X and Y values of every point in the mask.

## Vertical Bathtub

The V Bathtub allows the user to get the vertical Bathtub of a specific channel. The value entered in the textbox must be in ps, and according to the estimated time 2 s, the curve will be drawn. Also, the deep eye height can be entered to get the BER level.

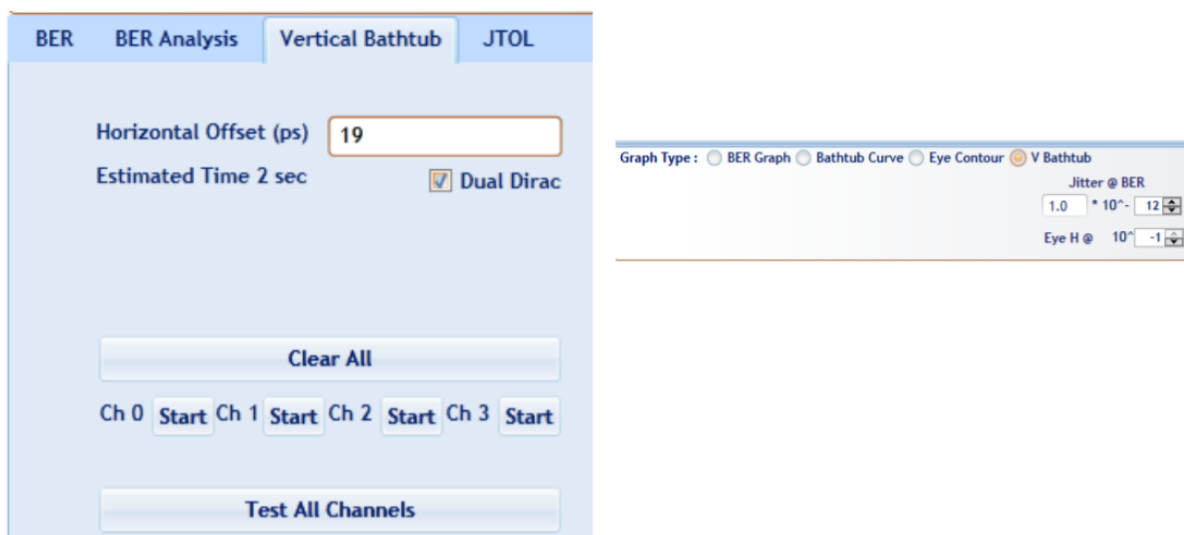


Figure 19 Vertical Bathtub

## Burst Mode

Burst mode allows the user to define the PPG signal and bits frequency. In order to enable Burst mode, ARB OUT is selected and AWG pattern is defined.

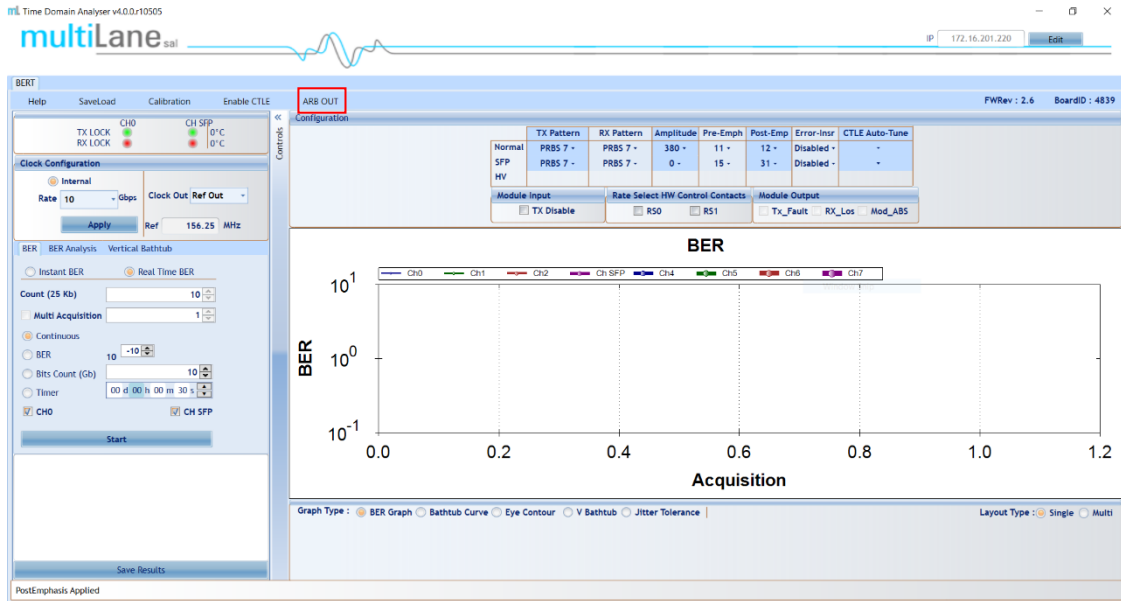


Figure 20 ARB OUT selection

ARB\_OUT

## AWG Burst Control Signal (TTL) 200 MHz max

AWG Pattern (64 bit user-defined pattern) hex values

0000000000000000

Bit Period  ns

Apply

Figure 21 Burst mode pattern and period window

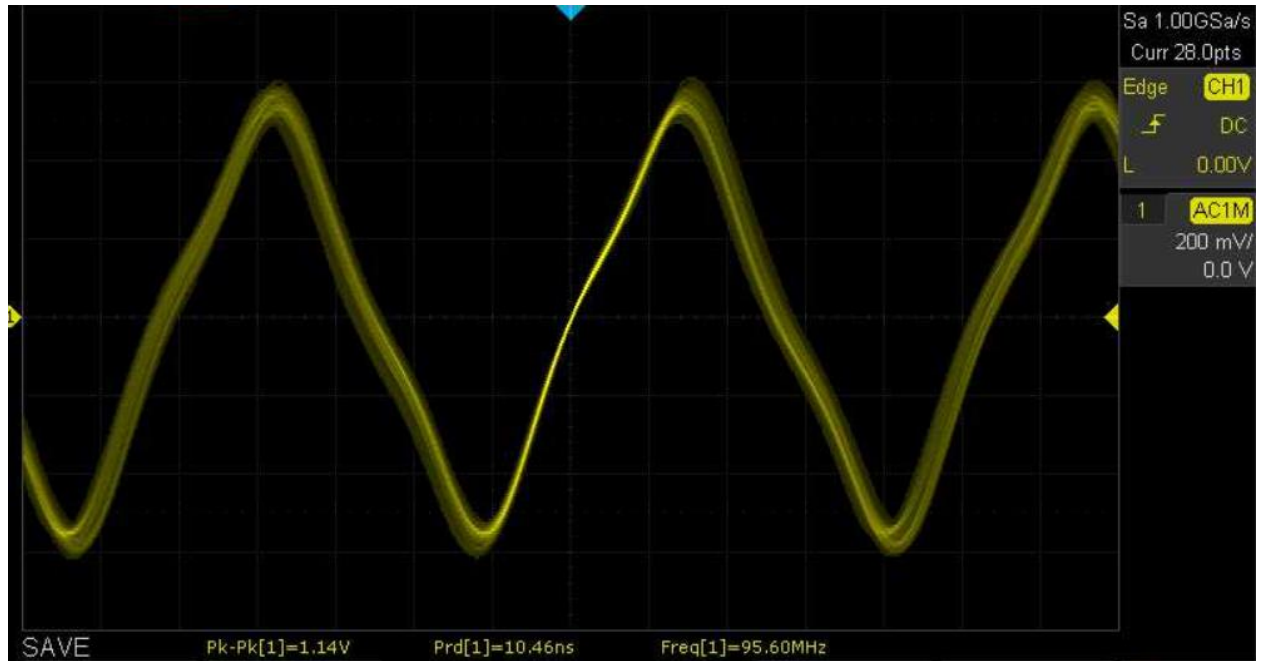


Figure 22 AAA AWG Pattern

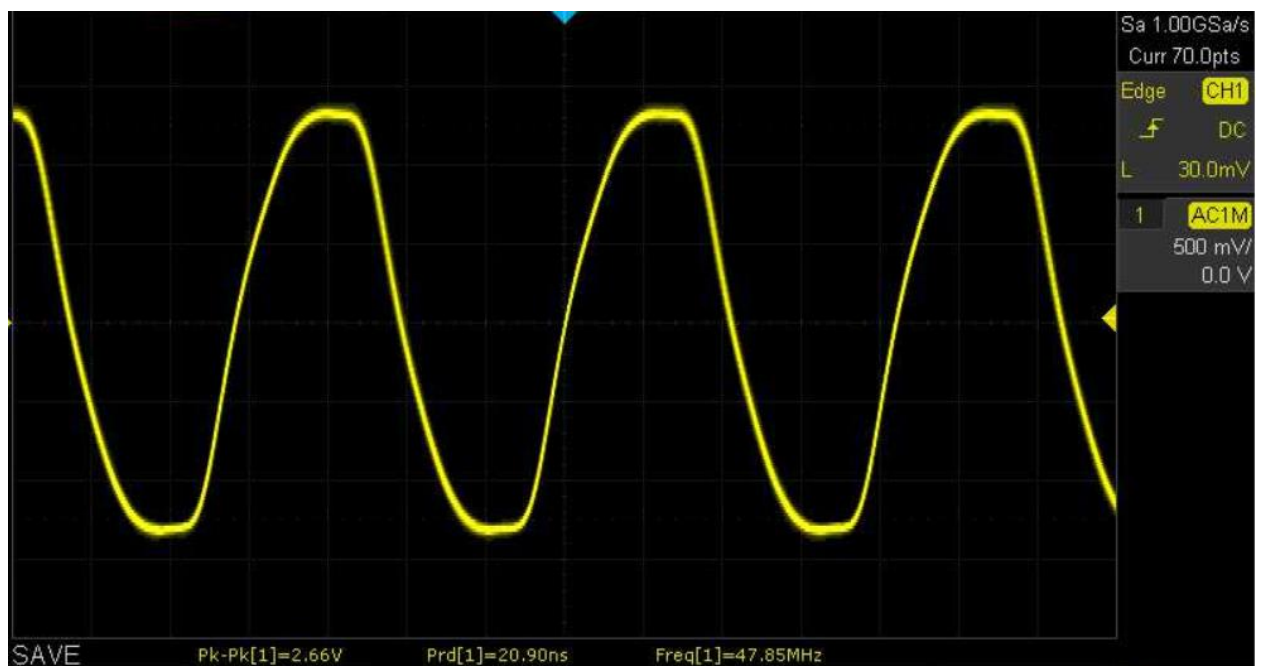


Figure 23 CCC AWG Pattern



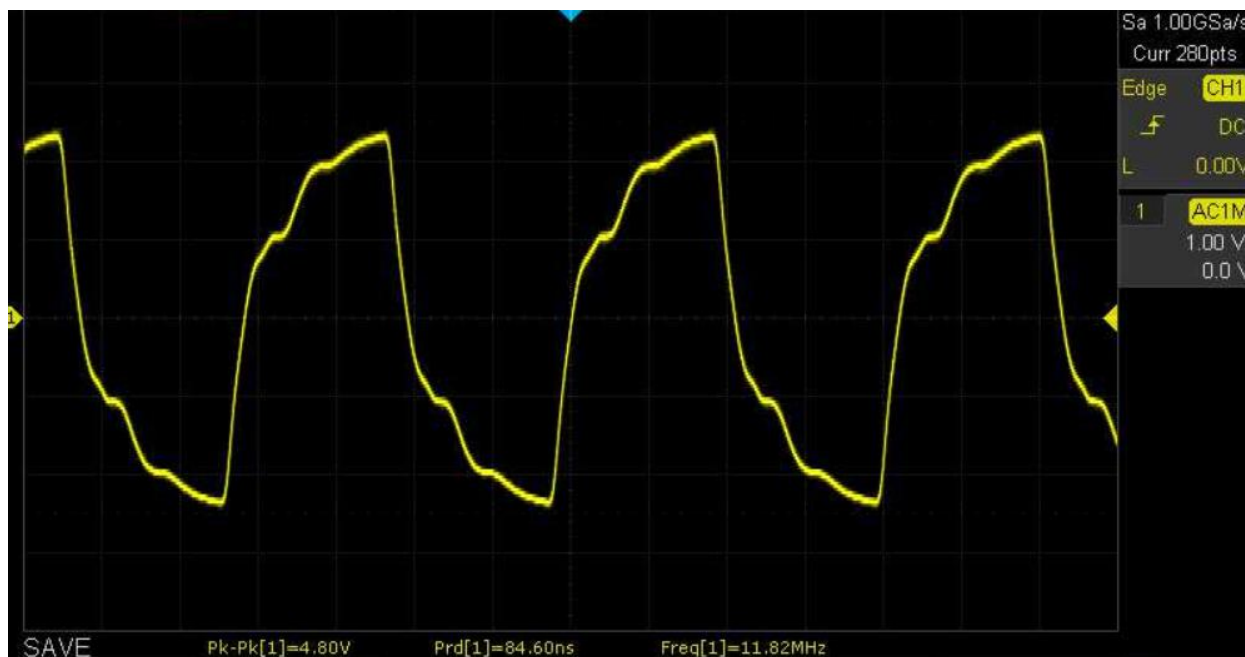


Figure 24 FF00 AWG Pattern

## DSO Configuration

In order to use ML4003BX as DSO, select DSO from the main window and click on configure.



Figure 25 DSO Configuration

## Clock Configuration

To configure the DSO Clock, the user can select:

- **External** if a clock source is connected to the CLK In pin.
- **Looped back from BERT** if the ML4003BX is used as a BERT and DSO simultaneously.
- **CDR** if the user wants to enable CDR option.

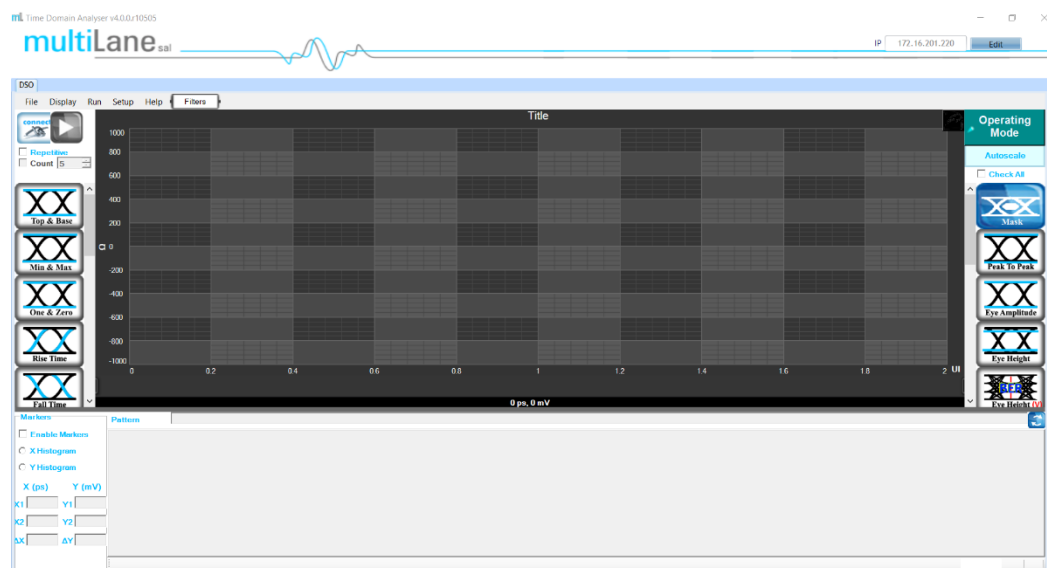


Figure 26 DSO GUI

## DSO GUI

- Click the connect button at the top left of your screen
- The “Connect to DSO” window will pop up
- Configure the DSO



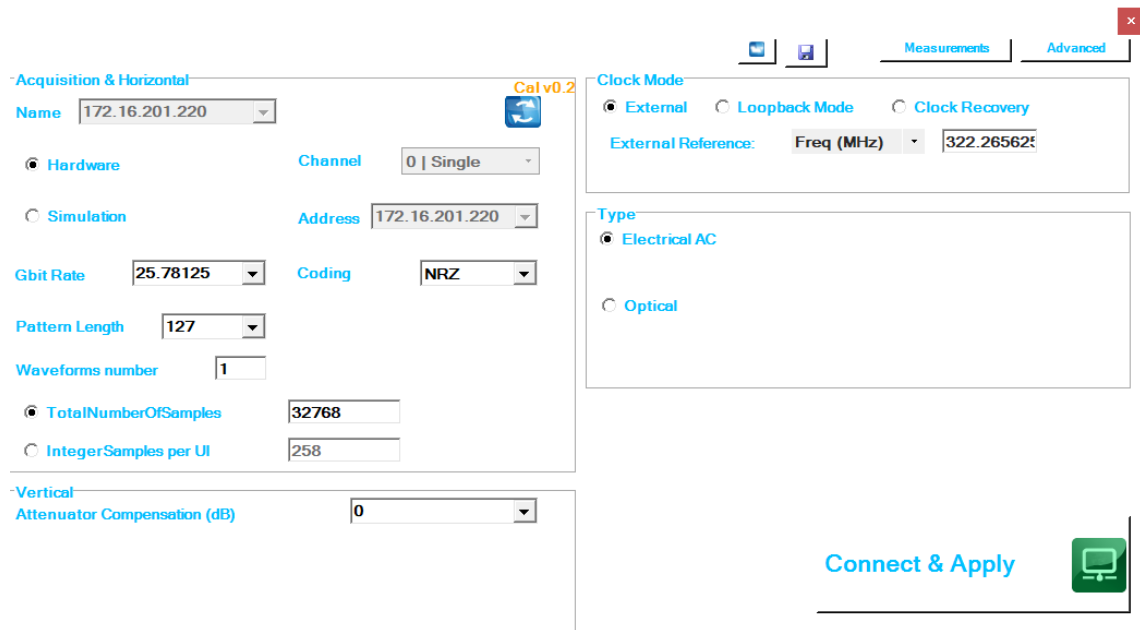


Figure 27 DSO Configuration window

- Set the Line Rate
- Enter the Pattern Length of the data feeding the DSO to capture the full pattern  
Note: Incorrect pattern length would still display the eye capture, however full pattern capture is required for certain features of the software such as Jitter Decomposition, PTB and Filters.  
E.G.: Pattern Length = 127 for PRBS-7, The Pattern length of PN(n) is  $(2^n) - 1$ .
- Specify clock mode:
  - **External** for external clock source. In this case, the frequency or rate should be set.
  - **Loopback mode** if the ML4003BX BERT is generating the signal.
  - **Clock Recovery** for CDR mode.
- Connect and apply.

\*For more details about DSO configuration refer to [this link](#)

## Operating Modes

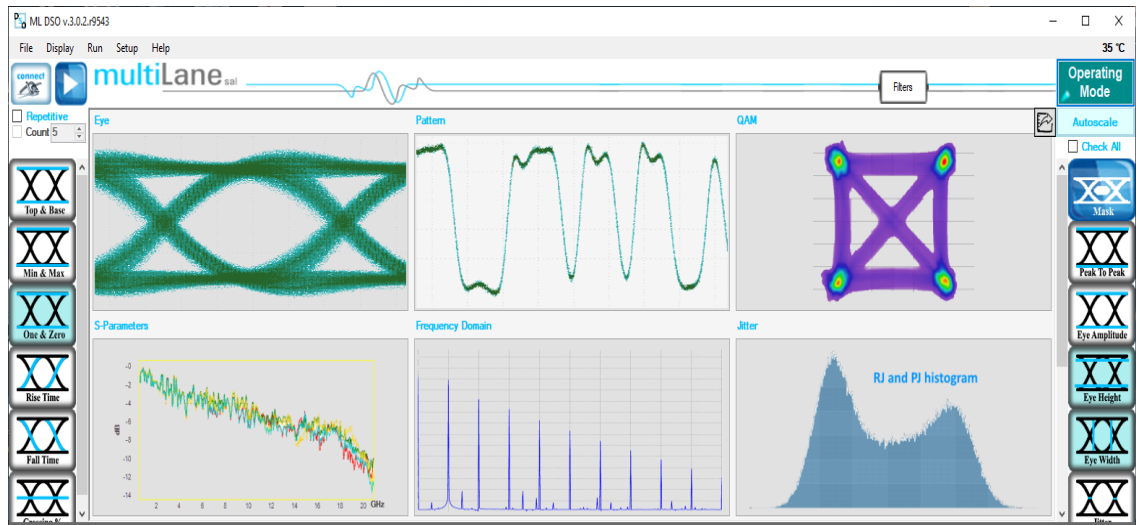



Figure 28 Operating modes

Selecting **Operating Modes** in upper right corner allows navigation between:

- Eye Measurement Mode:
  - Oscilloscope Measurements
  - Multiple measurements
  - NRZ Measurements
  - Mask Test
- Pattern Capture Mode including jitter decomposition
- S-Parameter Mode
- Frequency Domain Mode

## Eye Measurement Mode

Regardless of hardware or simulation mode, it is possible to draw the eye and capture measurements after filling the configuration window and connecting to the instrument.

In Eye Mode, in order to draw the eye diagram, click on the **Start Data Acquisition** button 

Check the **Check All** button to view all the eye measurements down the screen for one time or select the needed measurement only by pressing on the desired icons. Use the second option to reduce measurement operation time.

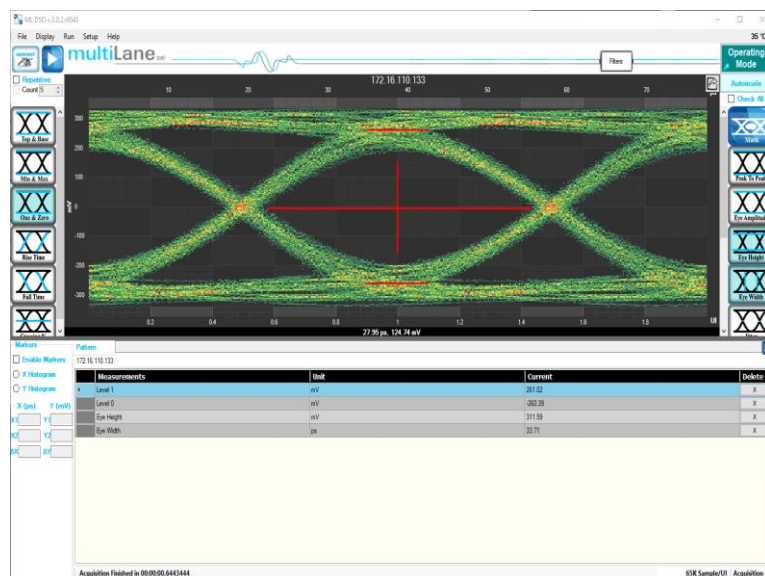


Figure 29 Eye diagram

## Filters

The DSO GUI platform comes equipped with useful filters that offer a variety of signal processing techniques including cleaning the signal, de-embedding and discovering the optimal taps for improving an NRZ signal. The filtering GUI can be used to adaptively detect the minimum number of FFE or DFE taps required to reach a target Eye Height or SNR.

These filters can be applied to a DUT signal with or without introducing the **preserve noise** feature, which compensates for the filter side effect of reducing signal noise of adjacent measurement points.

Click on the Filters button after a successful signal acquisition.

Current List of Supported Filters:

- 1- Moving Average Filter for signal smoothing: User can specify window size.
- 2- 4<sup>th</sup> Order Bessel Thomson filter at frequency equal to 0.75 of the bit rate (order and cutoff are configurable).

- 3- CTLE filter: User can automatically or manually select the filter parameters. Adaptive CTLE can determine the CTLE for best Eye Height.
- 4- S2P/S4P De-Embedding: This filter simulates the inverse of a channel or DUT, where the channel's S2P or S4P file is loaded. Can also emulate channel insertion loss.
- 5- DFE: The Decision Feedback Equalizer (nonlinear adaptive equalizer) is based on the principle that once the decision circuit has determined the value of the current transmitted symbol, one can precisely remove the ISI contribution of that symbol to future received symbols. Optimal DFE parameters can be determined by the GUI, and it can also adaptively detect minimum taps required for a target Eye Height or SNR value.
- 6- FFE: With the Feed Forward Equalizer (linear equalizer), each value of the output sequence is a weighted sum of the most recent input values. Optimal FFE parameters can be determined by the software, and it can also adaptively detect minimum taps required for a target Eye Height or SNR value.
- 7- SIRC: Also referred to as SRC, stands for System Impulse Response Correction. It is the extracted time domain impulse response of a reference O/E which is converted into the frequency domain using an FFT. Two methods with which this file is generated are discussed in detail in Appendix IV. Either method will yield a 4<sup>th</sup> Order Bessel-Thompson roll-off as dictated by the IEEE 802.3bs/cd publication standards for both NRZ and PAM4 optical signals.

*\*For more details about filters refer to [this link](#)*

## S Parameter Mode

The MultiLane DSO is now capable of measuring insertion loss S-parameters.

Depending on how the DSO is connected, the user should be able to measure either of S21 dd, S12 dd, S21, S12, S43, S34, etc.

The only difference between all the above is:

1. Single ended vs. differential connection.
2. The direction in which the DUT is connected for S-param capture.
3. The ports in use when connecting the DUT via a single ended connection.

The approach used consists of the following steps:

1. Define Circuits:
  - a. Main Circuit: Contains the DUT whose S-parameters are to be captured.
  - b. Reference Circuit:
    - i. Excludes the DUT whose S-parameters are to be captured.
    - ii. Is as identical as possible to the Main Circuit, except for the DUT.
    - iii. May require an additional component, such as a through, to be placed in the location of the DUT to close the circuit.

2. Set up the PPG:
  - a. PRBS 7 or 9, PRBS9 is recommended.
  - b. Maximum bit-rate possible (For maximum frequency range in the result)
  - c. Cleanest possible Eye: This sometimes translates to maximum amplitude to maximize SNR. However, be careful not to exceed the maximum amplitude supported by the MultiLane DSO without using attenuators.

**Kindly note PPG settings and amplitudes should not be altered after this point.**

3. Capture the reference signal: when having the optimal PPG settings as described above, and with the reference circuit connected, run the DSO S-Parameter Setup Wizard to capture reference data.
4. Without altering any of the PPG settings, connect the main circuit, simply connect the DUT where needed to switch from **Reference Circuit** to **Main Circuit**, and run in S-parameter mode, the S21 insertion loss result will be visible.

*For a constant PPG Source Signal, S21 Is calculated using the equation:*

*Frequency Response of DUT = FFT (Main Circuit Signal) / FFT (Reference Circuit Signal)*

5. Insertion loss can be saved in external .S21 or .DsoCirc files. These files contain both magnitude and phase information; however, phase information is not accurate in the sense that there will always be a linear shift in phase. These files with their magnitude and phase information can later be used in the DSO Software for de-embedding or DUT emulation.

## Components in Use

1. Two pairs of cables.
2. Two Module Compliance Boards that support the DAC connector. MCB S-parameters will be required. Often S-parameter information is supplied by the vendor.
3. One DAC cable.
4. Two through connectors that can mate the cable pairs together. These connectors will be considered to have negligible insertion loss.
5. MultiLane DSO
6. Any PPG, in this example the MultiLane BERT was used.

## First, Connect Your Reference Circuit Hardware

Begin with connecting the circuit you will use as reference circuit as follows:

Connect PPG differentially to Cable Pair 1, to Throughs, to Cable Pair 2, then to the DSO PPG => Cables 1 => Through => Cables 2 => DSO.

## Step 2, Configure your PPG for Cleanest Signal

1. Setup your PPG: Kindly refer to step 2 under “S Parameter Mode” found on page 30.
2. Observe the signal on the DSO after going through the ‘Reference Circuit’. Tune the PPG settings, sometimes you need to alter emphasis settings, sometimes amplitudes, sometimes bit rates. The cleanest eye possible for the highest rate possible will yield the most accurate result.
3. Once PPG settings are finalized, note them down. Kindly note PPG settings should not be altered after this point

## Step 3, Go Through the S-Parameter Wizard on the DSO

### Connect to the DSO

This DSO should currently be reading the signal going through the reference circuit. Recommended settings include a packet size of 512 and SW-PTB enabled.

### Go to S-Parameter Setup

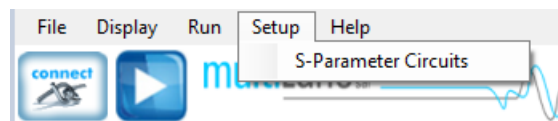
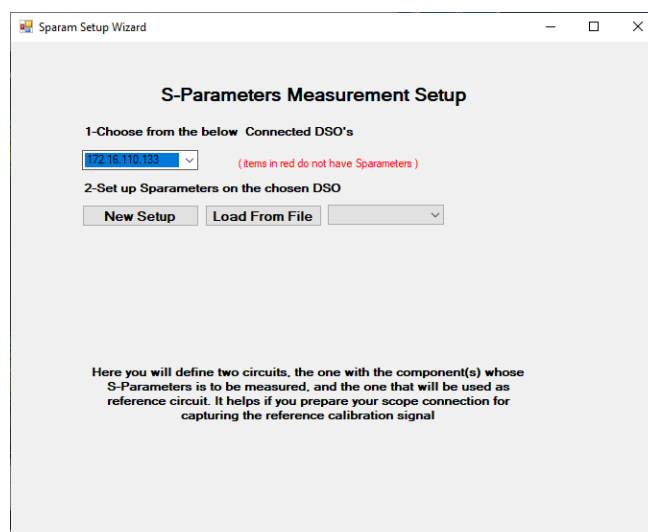


Figure 30 S-Param setup

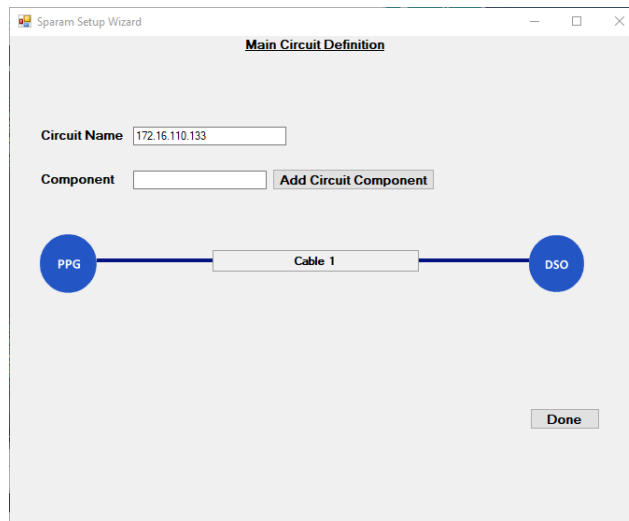
### Select the DSO Connected

After selecting the DSO click ‘New Setup’.



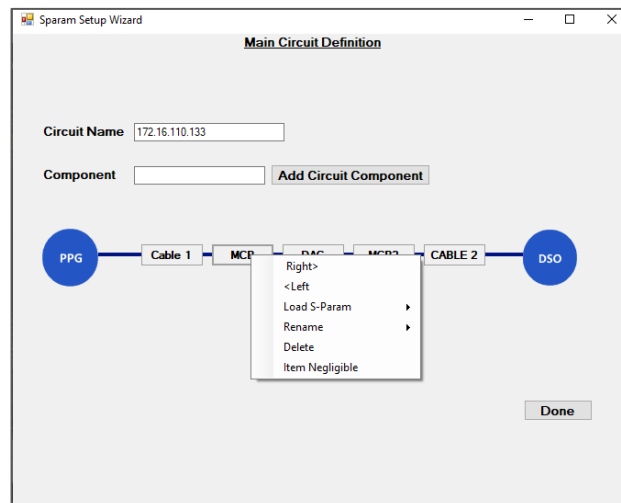


## Create Your Main Circuit



## Add the Main Circuit Components

Load the S-parameters of the MCBs. These will be used to calculate the S-parameters of the DAC DUT.

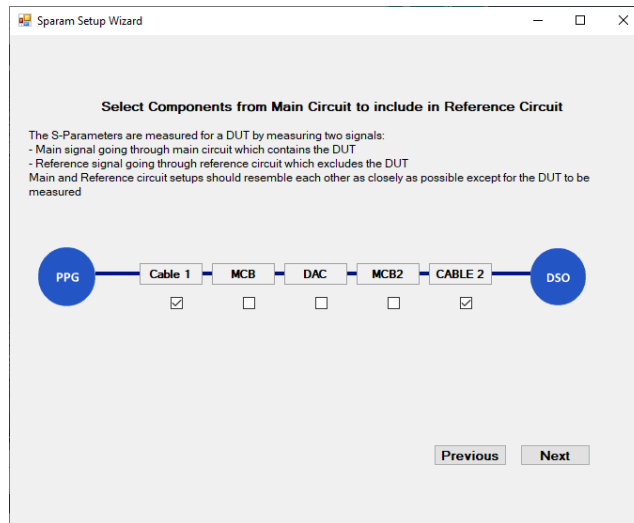


Proceed by clicking 'Done'.

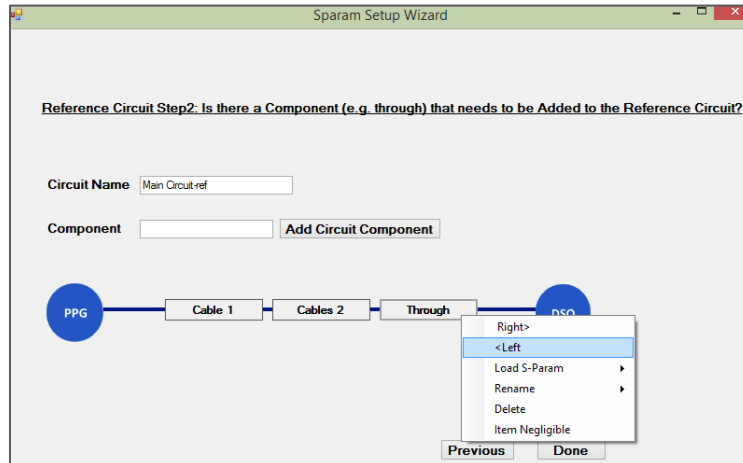
## Select Components from Main Circuit Present in Reference Circuit

Select Cables 1 and 2 and click Next.

## Add Through Connector in Reference Circuit Definition

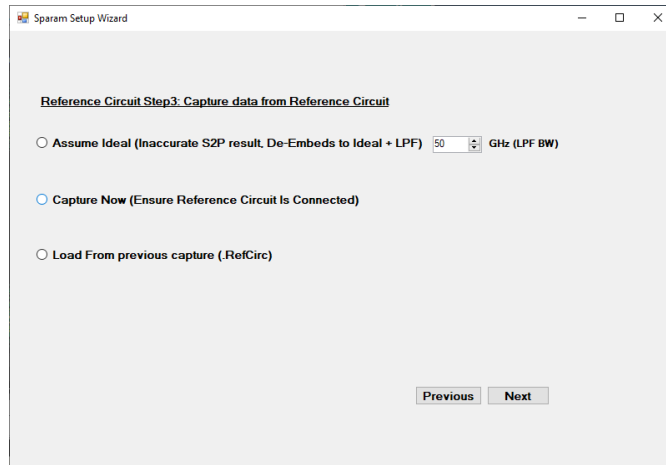


When done, click next.



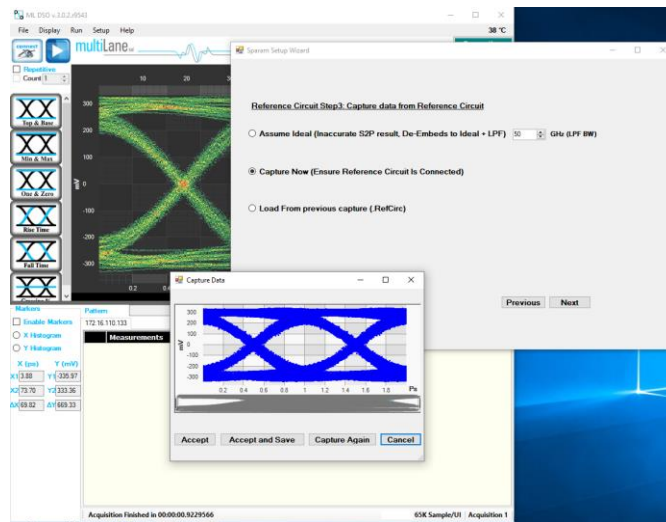
## Capture Reference Data

Click 'Capture Now'

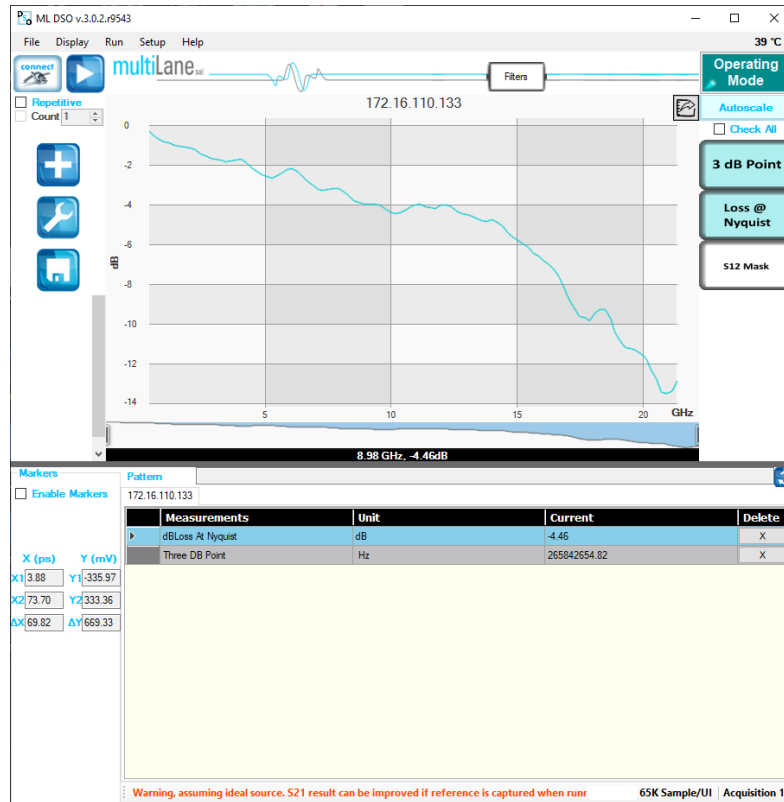


The captured eye is depicted, the user can accept it or recapture.

Alternatively, the user may 'Accept and Save' the reference eye data. This will save the captured reference data for future use, allowing the user to call on 'Load from. RefCirc' in the future when visiting this page, hence avoiding reconnecting the reference circuit.



Click 'Next'



## Frequency Domain Mode

Upon moving to frequency domain mode, the frequency response can be plotted, and the total harmonic distortions can be calculated.

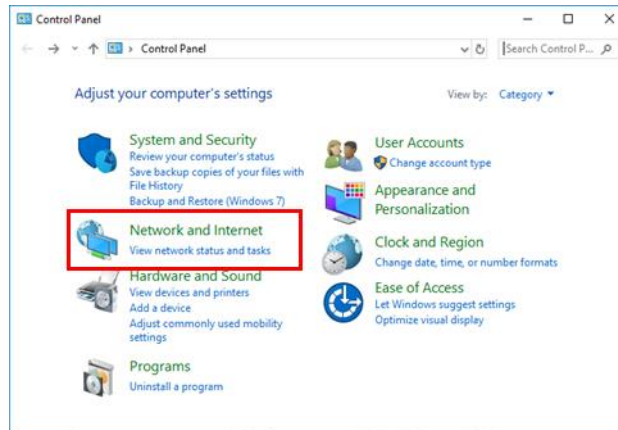




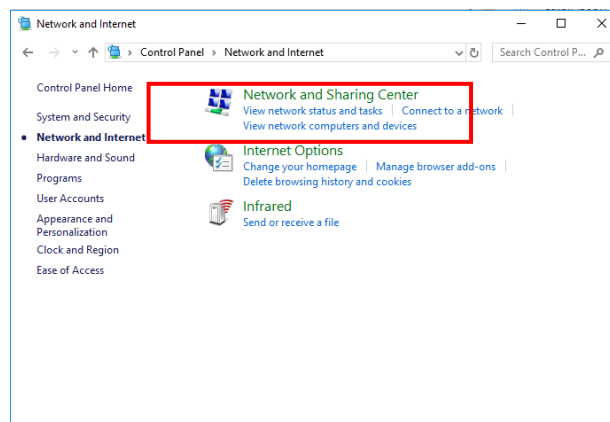
## Appendix 1 – Adding the ML4003BX to the Network

To create a local network connection, please follow these steps:

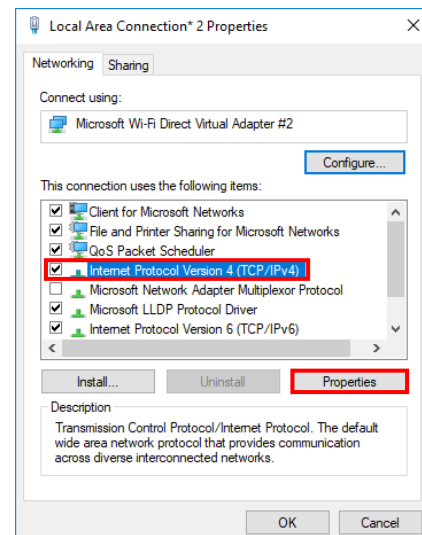
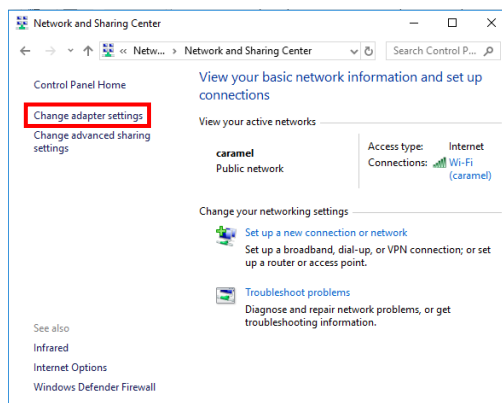
- **Create a local network connection** between the laptop and the ML4003BX using Internet Protocol Version 4 (TCP/IPv4).
  - **Open “Control Panel”** and **choose “Network and Internet”**.
  - **Open “Network and Sharing Center”**.



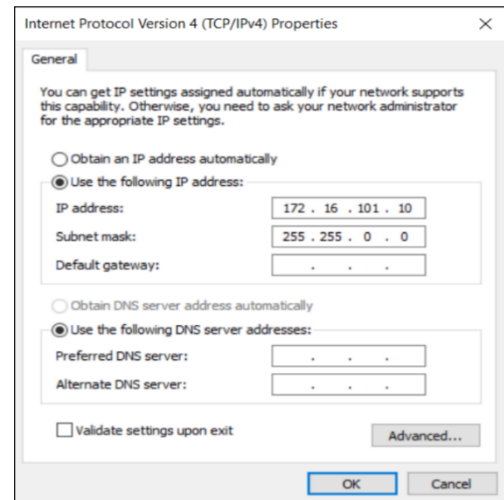
- **Click on “Change Adapter Settings”,** then **choose “Local Area Connection”**.



- In the Networking Tab, **click on “Internet Protocol Version 4 (TCP/IPv4)”** then **“Properties”**.



- **Add a similar IP Address** that shares a subnet with the instrument IP in the Advanced tab. This will be used to ping the instrument once the IP Address is changed to match that of the network.
- **Connect the laptop** directly to the ML4003BX using an Ethernet cable.
- **Copy the IP Address** found on the back of the unit.
- **Ping the device** to make sure that the connection is successful.
- Now a new local network has been successfully defined.



**NOTE:**

These steps are illustrated using Windows 10. Kindly note that previous versions of Windows have a similar procedure with slight differences in tabs or folders' names.





**North America**

48521 Warm Springs Blvd.  
Suite 310  
Fremont, CA 94539, USA  
+1 510 573 6388

**Worldwide**

Houmal Technology Park  
Askarieh Main Road  
Houmal, Lebanon  
+961 81 794 455

**Asia**

7th Floor-2, No. 156  
Sec. 2, Dongda Road, North District,  
Hsinchu City 300, Taiwan (R.O.C.)  
+886 3 5744 591

**UAE**

Building 4WA, Office 420  
Dubai Airport Freezone Authority,  
Dubai, UAE  
+971 4 548 7 547